

REMARKS

Claims 1-7 and new claims 13-18 are now in this application. Claims 1-12 are rejected. Claims 8-12 are objected to and cancelled. Claims 1-7 are amended herein to clarify the invention, to broaden language as deemed appropriate and to address matters of form unrelated to substantive patentability issues.

Applicants respectfully request that the Examiner acknowledge receipt of the priority document filed in this application on April 10, 2002.

Claim Objections

Claims 8-12 are objected to under 37 C.F.R. §1.75(c) as being of improper dependent form.

Claims 8-12 are canceled so the Examiner's objection to these claims has been rendered moot.

Claim Rejections-35 U.S.C. §112

Claims 8-12 are rejected under 35 U.S.C. §112, second paragraph.

Claims 8-12 are canceled so the Examiner's rejection of these claims has been rendered moot.

Claim Rejections-35 U.S.C. §102

Claims 1 and 4-7 are rejected under 35 U.S.C. §102(e) as being anticipated by Hsu et al. (U.S. Patent No. 6,462,366).

The Examiner's rejection is respectfully traversed in view of amended claim 1. Claim 1 is amended to clarify that the first insulator film substrate extends "over the entire channel region" of the semiconductor substrate which is between a source region and a drain region such that the first insulator film completely separates the semiconductor substrate from the first conductor layer. As shown in Fig. 1, the first insulator layer 3 extends over all of the channel region 2 in contact therewith to separate the first conductor layer 4 from the semiconductor substrate 1. Thus, the invention relates to an MFMIS (Metal - Ferroelectric - Metal - Insulator - Semiconductor) structure (in order from the top, the second semiconductor layer 6-metal, the ferroelectric layer 5-ferroelectric, the first conductor layer 4-metal, the first insulator layer 3-insulator, the substrate-semiconductor).

In contrast to the invention, Hsu et al. '366 relates to an MFMS (Metal - Ferroelectric - Metal - Semiconductor) structure (in order from the top, top electrode 100 -metal, ferroelectric material 98-ferroelectric, bottom electrode 96-metal, n-layer 86 of substrate 82-semiconductor). Thus, in Hsu et al. '366, there is no insulator layer between the entire bottom electrode 96 and the semiconductor substrate 86 and the MFM structure is formed directly onto the semiconductor

substrate 86, i.e., the bottom electrode 96 is in direct contact with and connected to the semiconductor substrate 86. The insulating layer 88 extends over only a portion of the n-layer 86 and does not extend over the entire n-layer.

In view of the connection between the bottom electrode 96 (the first conductor) and the semiconductor substrate 86 in Hsu et al. '366, the drain of the first conductor and the source are connected and thus it does not function as a field effect transistor type ferroelectric nonvolatile storage element. By contrast, by providing the first insulating layer between the channel region of the semiconductor substrate and the first conductor layer, a complete separation of the first conductor layer from the semiconductor substrate is provided. This MFMIS - FET type memory functions as a field effect transistor type ferroelectric nonvolatile storage element by the polarization of the ferroelectric body changing the threshold voltage of the transistor, the change in resistance of the channel between the source and drain being readable as a change in the magnitude of drain current value. Therefore, the function and effect of the invention is clearly different from that of the Hsu et al. '366 invention.

Also, Hsu et al. does not teach or suggest extending the insulating layer 88 over the entire n-layer 86 as this would frustrate the purposes of the Hsu et al. device and fundamentally change the operation and of the Hsu et al. device.

In view of the foregoing, Hsu et al. '366 does not disclose a semiconductor storage element including all of the features of claim 1 and therefore cannot anticipate the embodiment of the invention set forth in claim 1.

Claims 4-7 depend from claim 1 and necessarily include all of the features thereof. For the same reasons that claim 1 is patentable over Hsu et al. '366, claims 4-7 should also be patentable over Hsu et al. '366.

Claim Rejections-35 U.S.C. §103

Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hsu et al. '366 in view of Fukuzumi (U.S. Patent No. 6,403,444).

Fukuzumi does not disclose an insulator layer arranged over the entire channel region of a semiconductor substrate in an MFMIS type of semiconductor storage element and therefore one could not combine the Hsu et al. and Fukuzumi references and arrive at the embodiment of the invention set forth in claim 2.

Claim 3 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hsu et al. '366 in view of Hsu et al. (U.S. Patent No. 6,146,904).

Hsu et al. '904 does not disclose an insulator layer arranged over the entire channel region of a semiconductor substrate in an MFMIS type of semiconductor storage element and therefore one could not combine the Hsu et al. '366 and Hsu et al. '904 and arrive at the embodiment of the invention set forth in claim 3.

In view of the changes made to claim 1 and the arguments presented above, it is respectfully submitted that the Examiner's rejections of the claims have been

overcome and should be removed and that the application is now in condition for allowance.

New claims

Claims 13-18 are added and recite additional features of the storage element of claim 1. For example, claim 13 recites that the first insulator layer and the second insulator thin film form a U-shaped insulator as shown in Fig. 1. Claim 14 relates to the total effective area of the MIS structure and MIM structure, which feature is described in the specification in the paragraph bridging pages 23 and 24. Claim 15 recites that the first insulator layer and the second insulator thin film are formed at the same time (the embodiment shown in Fig. 1) while claim 16 recites that the second insulator thin film is formed separately from the first insulator layer (the embodiment shown in Fig. 3). Claims 17 and 18 recite features included in original claim 2. No new matter is introduced by the presentation of new claims 13-18.

Applicant respectfully requests a one month extension of time for responding to the Office Action. Please charge the fee of \$110 for the extension of time to Deposit Account No. 10-1250.

In light of the foregoing, the application is now believed to be in proper form for allowance of all claims and notice to that effect is earnestly solicited. Please charge any deficiency or credit any overpayment to Deposit Account No. 10-1250.

Respectfully submitted,

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